

IN THE CLAIMS

Please cancel claims 1-8, 16-17 and 19-20.

Please amend the claims as follows.

1-8 (Cancelled)

- 1 9. (Currently amended) An integrated circuit comprising:
 - 2 a register file bit comprising:
 - 3 a primary latch having a data input and a data output;
 - 4 a plurality of secondary latches each having a data input and a data output;
 - 5 a feedback path from the data ~~output~~ outputs of the plurality of secondary latches to the data input of the first ~~primary~~ latch, the feedback path including a data selection mechanism for selecting one data output only from among each of ~~the data outputs~~ from the plurality of secondary latches to feed back to the data input of the first ~~primary~~ latch; and
 - 6 a context switch mechanism that causes the data on the data output of the primary latch to be written to a selected one of the plurality of secondary latches, and that causes the data on the data output of the selected one secondary latch to be written to the primary latch.
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 - 1 10. (Original) The integrated circuit of claim 9 wherein the context switch mechanism comprises a swap signal coupled to the primary latch.
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 - 1 11. (Original) The integrated circuit of claim 9 wherein the context switch mechanism comprises a delay element between the data output of the primary latch and the data inputs of the plurality of secondary latches.
 - 2
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- 1 12. (Original) The integrated circuit of claim 9 wherein the context switch mechanism
- 2 comprises a delay element in the feedback path.

- 1 13. (Original) The integrated circuit of claim 9 wherein the context switch mechanism
- 2 comprises at least one clock signal that latches data on the data input of the primary latch
- 3 to the data output of the primary latch and at least one clock signal that latches data on the
- 4 data input of a secondary latch to the data output of the secondary latch.

- 1 14. (Original) The integrated circuit of claim 9 further comprising a plurality of write
- 2 ports on the data input of the primary latch.

- 1 15. (Original) The integrated circuit of claim 9 further comprising a plurality of read ports
- 2 on the data output of the primary latch.

16-20 (Cancelled)

- 1 21. (Currently amended) A method for performing a fast context switch in a register file
- 2 that includes a primary latch and a plurality of secondary latches having data outputs, the
- 3 method comprising the steps of:
 - 4 (A) for each of the plurality of secondary latches, performing the steps of:
 - 5 (A1) storing a value in the primary latch that corresponds to a selected
 - 6 thread;
 - 7 (A2) moving the value in the primary latch to a secondary latch;
 - 8 (B) storing a value in the primary latch that corresponds to an active thread;
 - 9 (C) selecting one data output only from among each of the data outputs of the
 - 10 secondary latches for performing a context switch with the primary latch; and
 - 11 (D) performing a context switch between the primary latch and the selected one
 - 12 secondary latch that causes the value in the primary latch to be stored in the selected one
 - 13 secondary latch, and that causes the value in the selected one secondary latch to be stored
 - 14 in the primary latch.
 - 1 22. (Original) The method of claim 21 wherein the context switch performed in step (D)
 - 2 occurs in a single clock cycle.

STATUS OF THE CLAIMS

Claims 1-22 were originally filed in this patent application. In the pending office action, claim 9 was objected to for an informality and claims 1-17 and 19-22 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,831,623 to Terzian. No claim was allowed. In the first response dated 04/20/2006, claims 1, 8, 16, 19 and 21 were amended and claim 18 was cancelled. A second response dated 08/02/2006 was not entered by the examiner. In this response, claims 9 and 21 have been amended and claims 1-8, 16-17 and 19-20 have been cancelled. Claims 9-15 and 21-22 are currently pending.